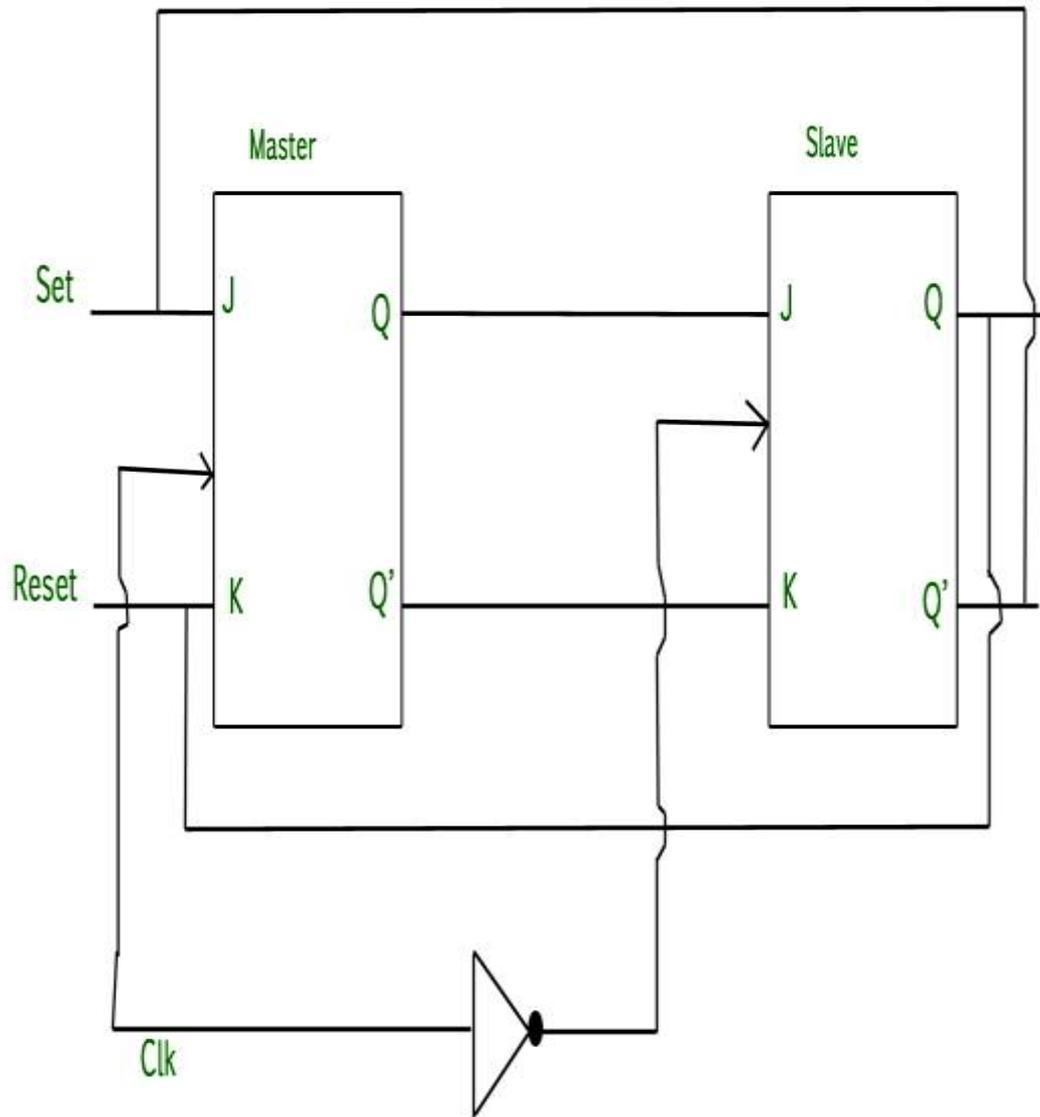


Race Around Condition In JK Flip-flop – For J-K flip-flop, if $J=K=1$, and if $clk=1$ for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop. This problem (Race Around Condition) can be avoided by ensuring that the clock input is at logic “1” only for a very short time. This introduced the concept of **Master Slave JK** flip flop.

Master Slave JK Flip Flop

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the “**master**” and the other as a “**slave**”. The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.

In addition to these two flip-flops, the circuit also includes an **inverter**. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop. In other words if $CP=0$ for a master flip-flop, then $CP=1$ for a slave flip-flop and if $CP=1$ for master flip flop then it becomes 0 for slave flip flop.



Master-slave JK Flip-Flop

Working of a master slave flip flop –

When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.

Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.

If $J=0$ and $K=1$, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.

If $J=1$ and $K=0$, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.

If $J=1$ and $K=1$, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.

If $J=0$ and $K=0$, the flip flop is disabled and Q remains unchanged.

If $J=0$ and $K=1$, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.

If $J=1$ and $K=0$, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.

If $J=1$ and $K=1$, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.

If $J=0$ and $K=0$, the flip flop is disabled and Q remains unchanged